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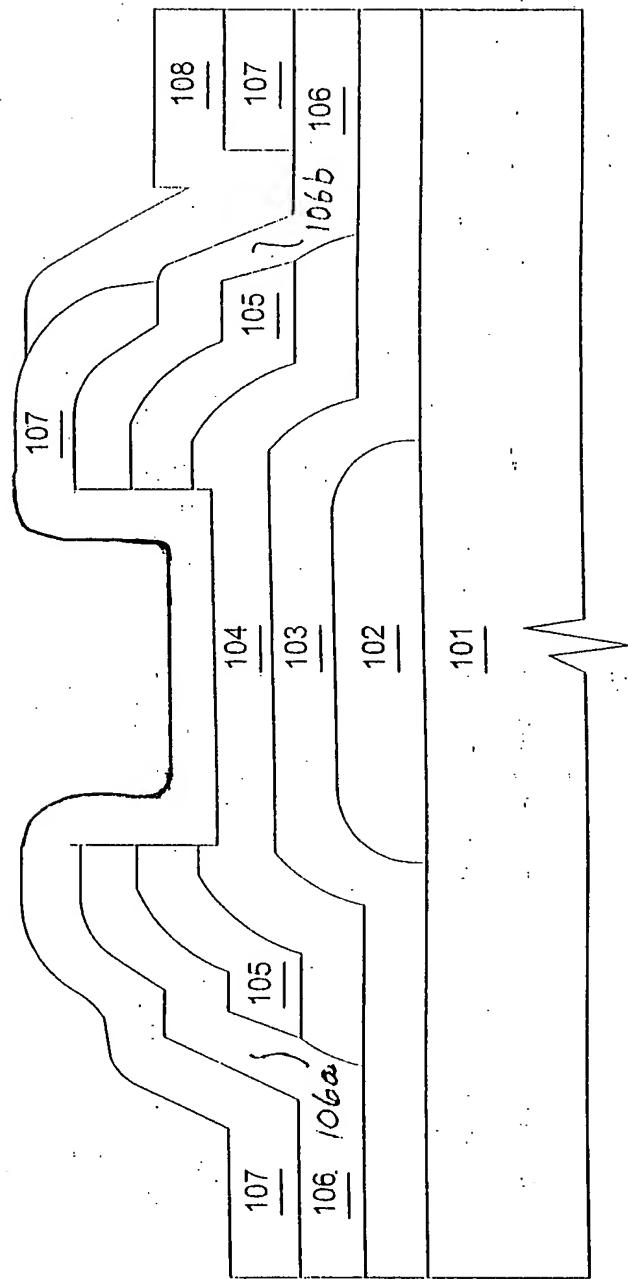


FIG. 1 (Prior Art)

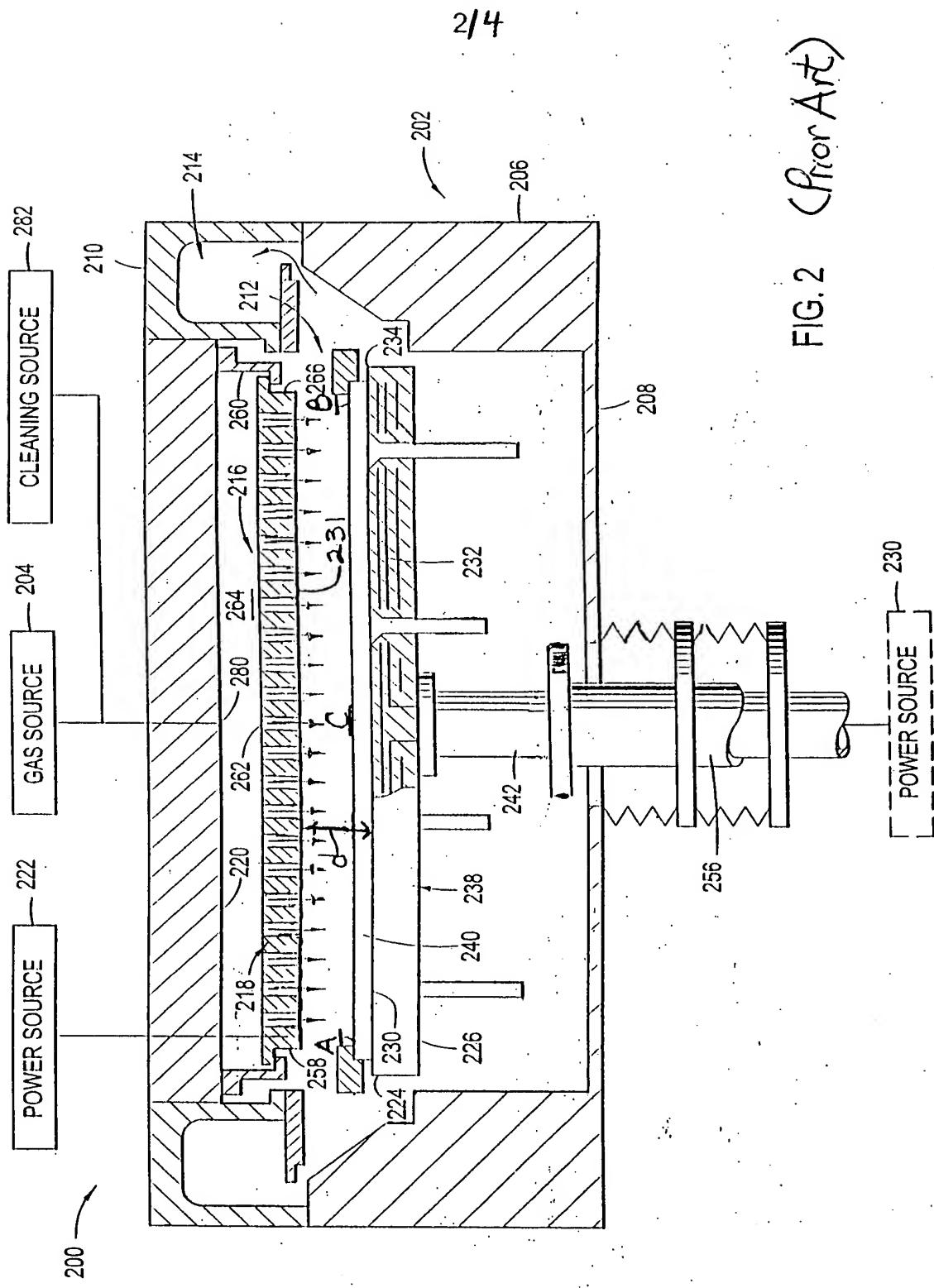


FIG. 2 (Prior Art)

ITO Pattern(MASK5)
 ITO Sputtering
 Passivation Etch (MASK4)
 SiNx PECVD
 n+a-Si Etch-Back
 S/D Pattern(MASK3)
 S/D Sputtering
 a-Si Pattern(MASK2)
 n+a-Si/a-Si/SiNx PECVD
 Gate Pattern(MASK 1)
 Gate Metal Sputtering

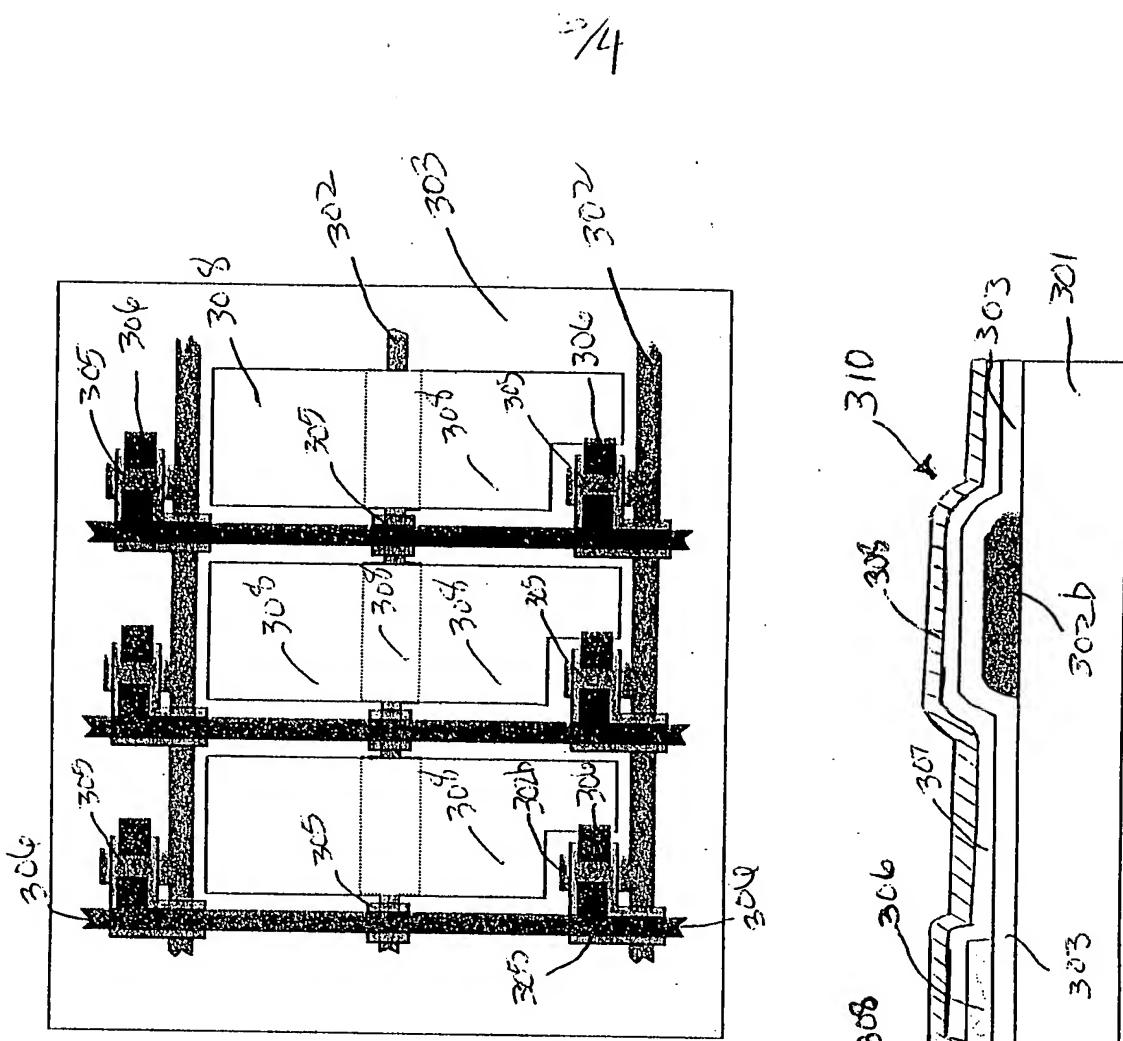


Fig. 3

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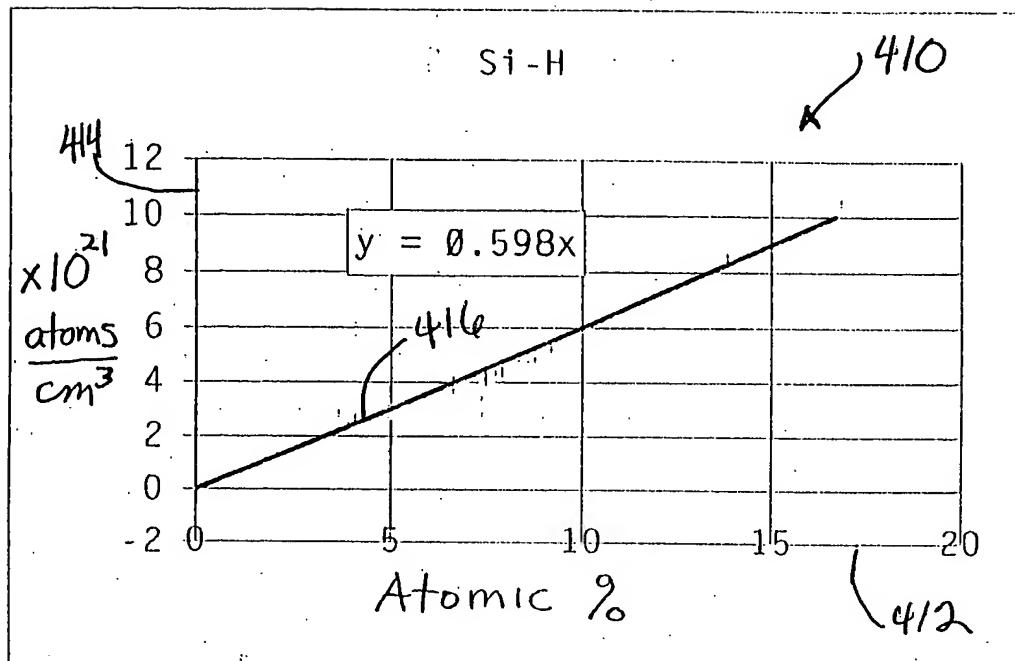


Fig. 4A

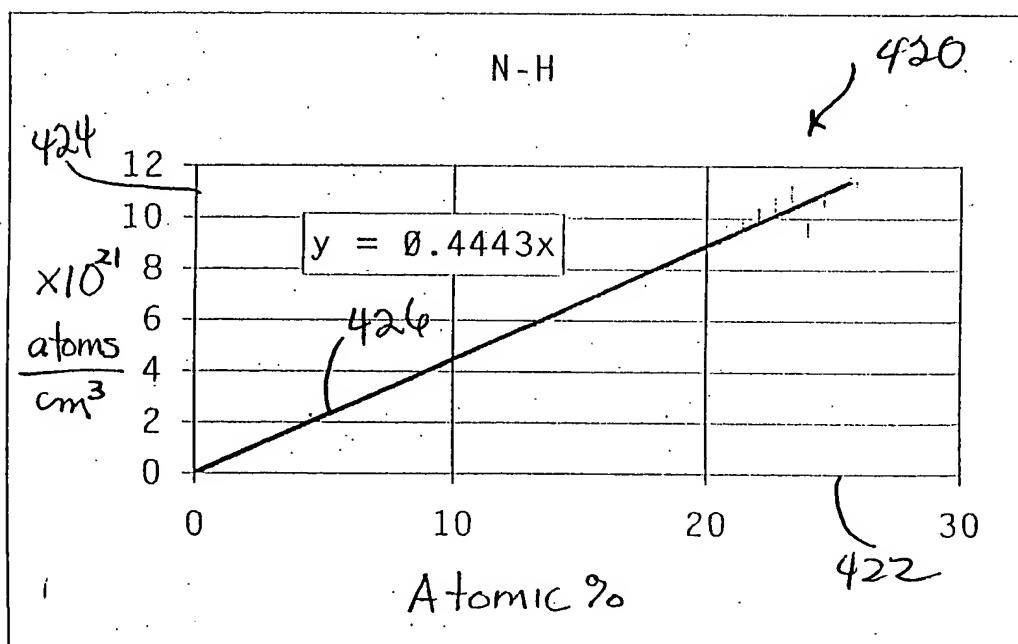


Fig. 4B